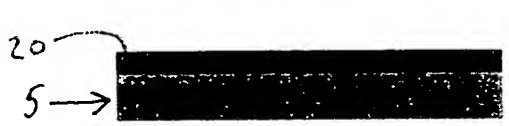
As grown wafer

FIG. 1A

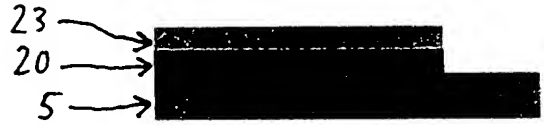


Sputter SiO2

FIG. 1B

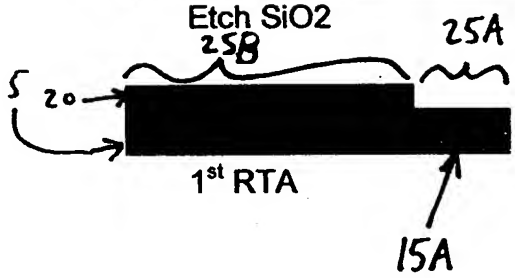
Photoresist patterning

FIG. 1C



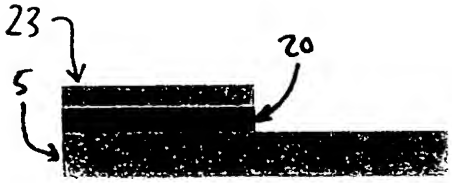
Etch SiO2

FIG. 1D



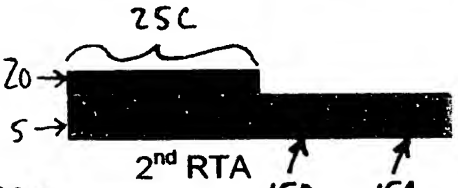
1st RTA

FIG. 1E



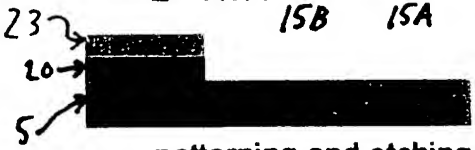
patterning and etching

FIG. 1F



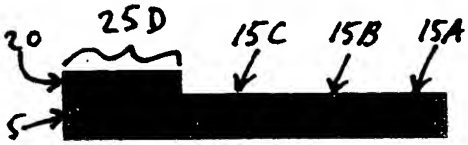
2nd RTA

FIG. 1G



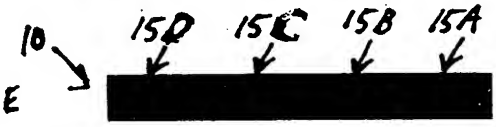
patterning and etching

FIG. 1H



3rd RTA

FIG. 1I



wafer for further process

FIG. 1J

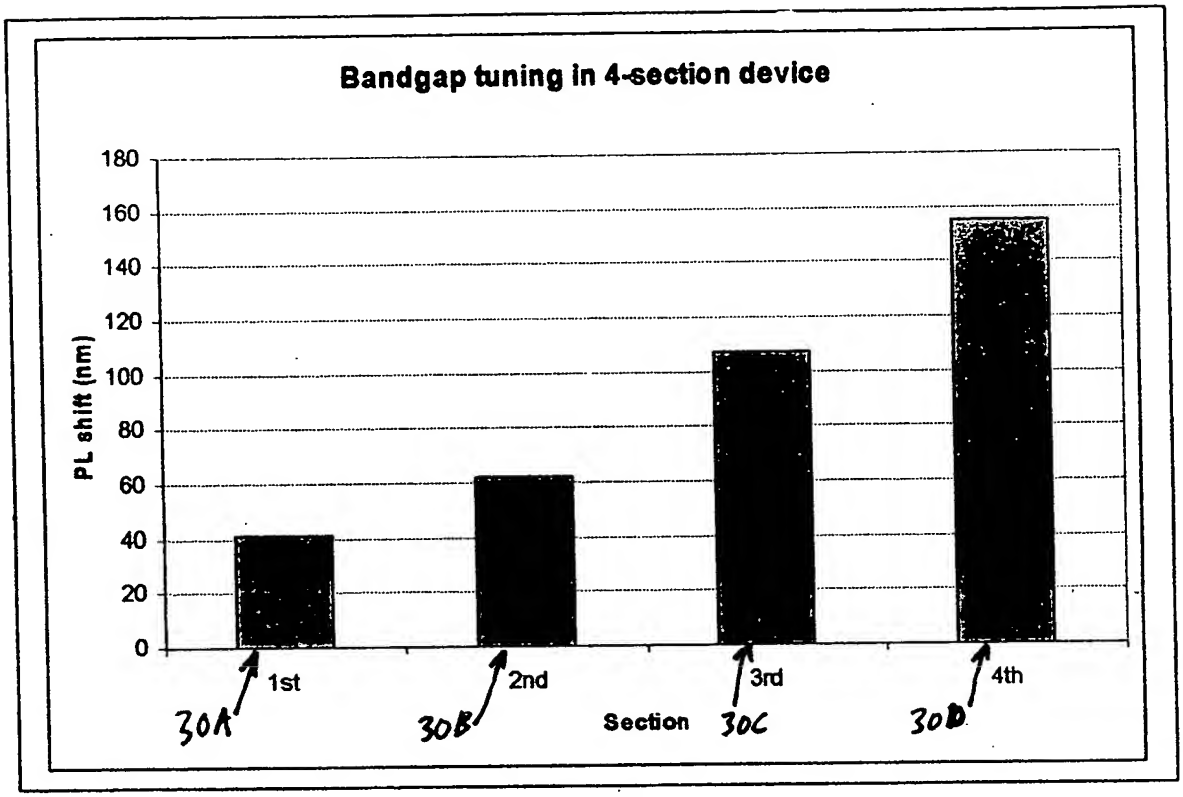


Figure 2

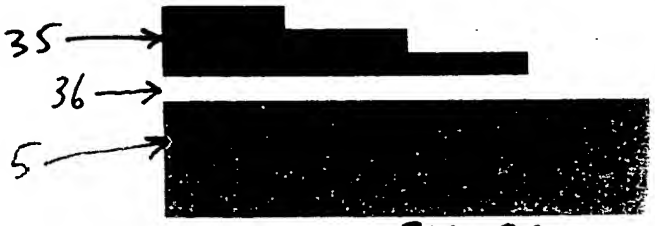


FIG. 3A

(a) patterning of the as-grown wafer

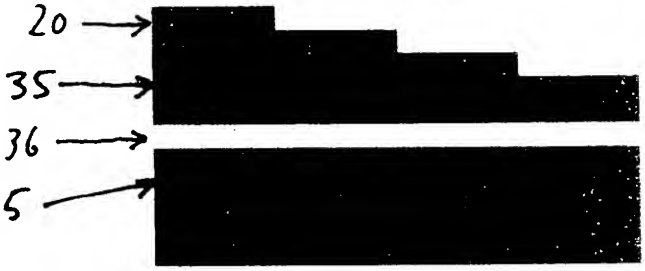


FIG. 3B

(b) patterning of the as-grown wafer , dielectric cap deposition and RTA

FIG. 3C

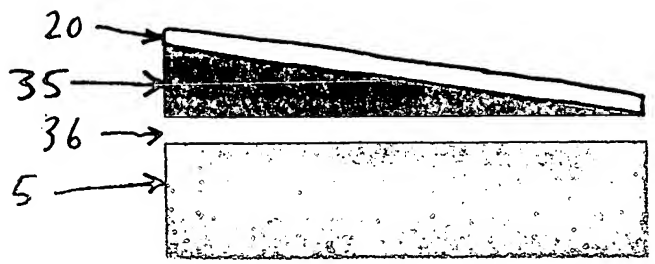
(c) remove all sacrificial layers for further processing of the device wafer

Device wafer

sacrificial layer

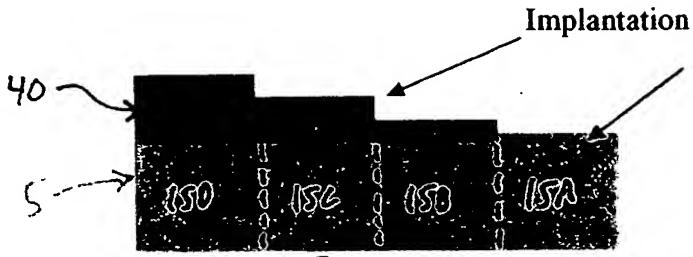
Etch stop

Dielectric cap



Device wafer | sacrificial layer | Etch stop | Dielectric cap

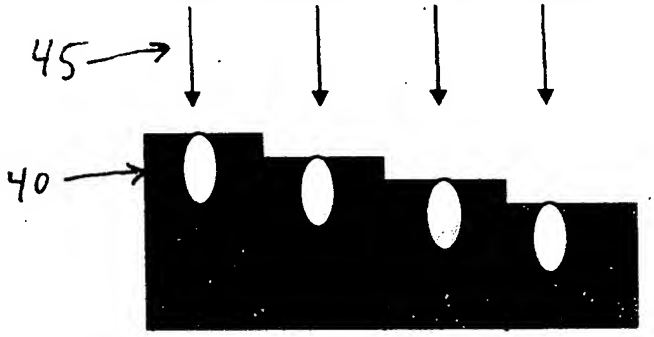
Figure 4



(a) patterning of varying implantation mask

FIG. 5A

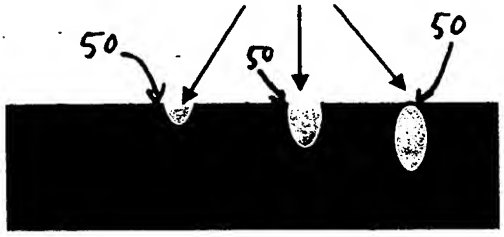
Implantation flux (uniform dosage & energy)



(b) patterning of the as-grown wafer , dielectric cap deposition and RTA

FIG. 5B

Left-over implantation damage in semiconductor



(C) spatially varied implantation damage that would lead to varying degree of disordering after RTA step.

FIG. 5C

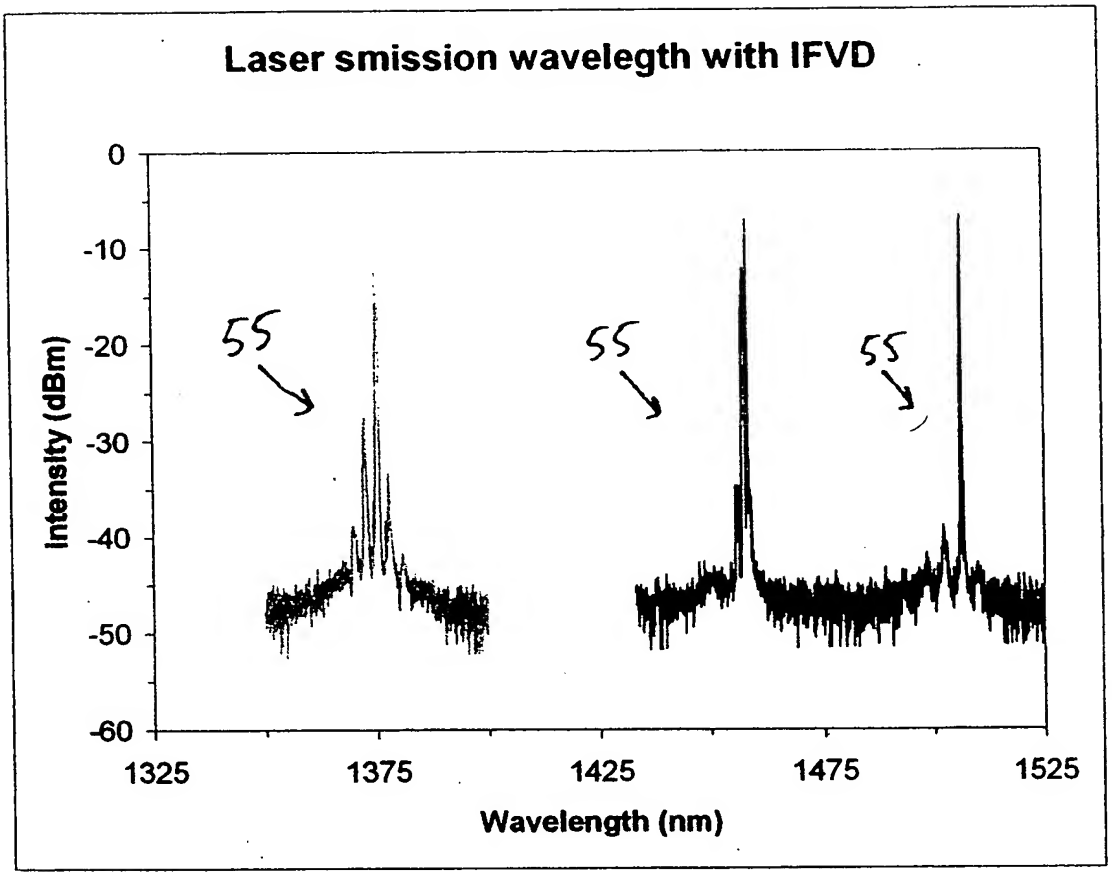


FIG. 6

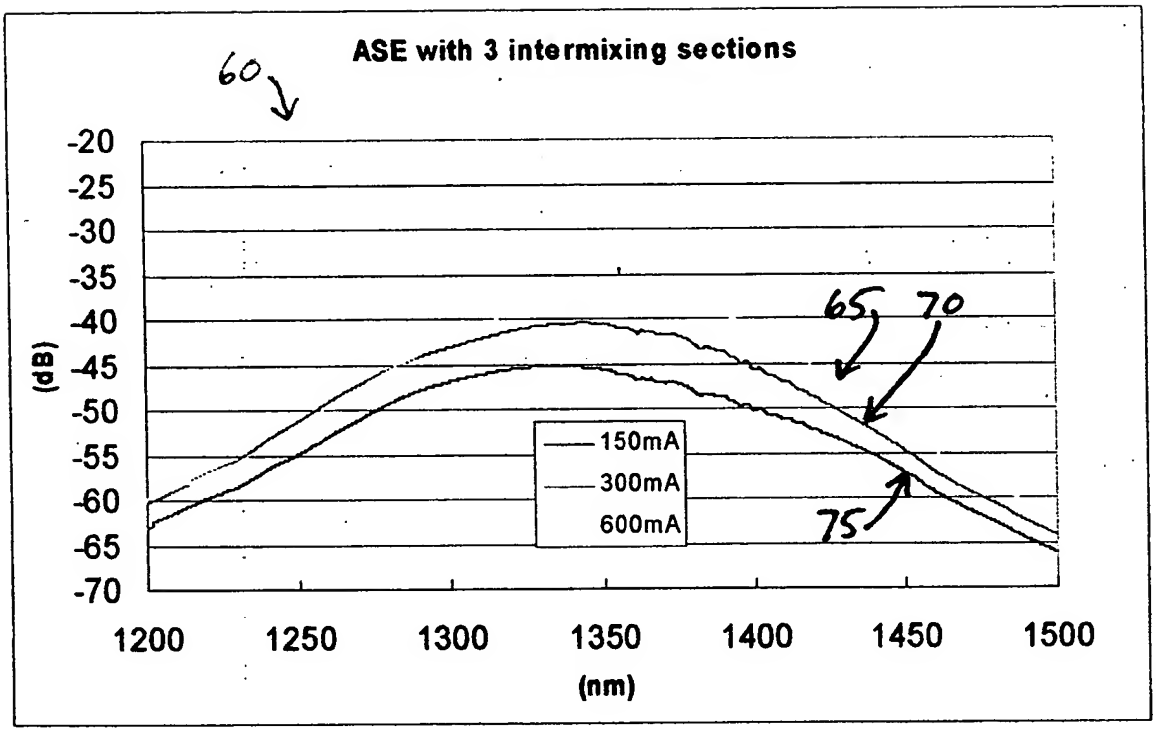


FIG. 7

KT/AHURA10.DRW

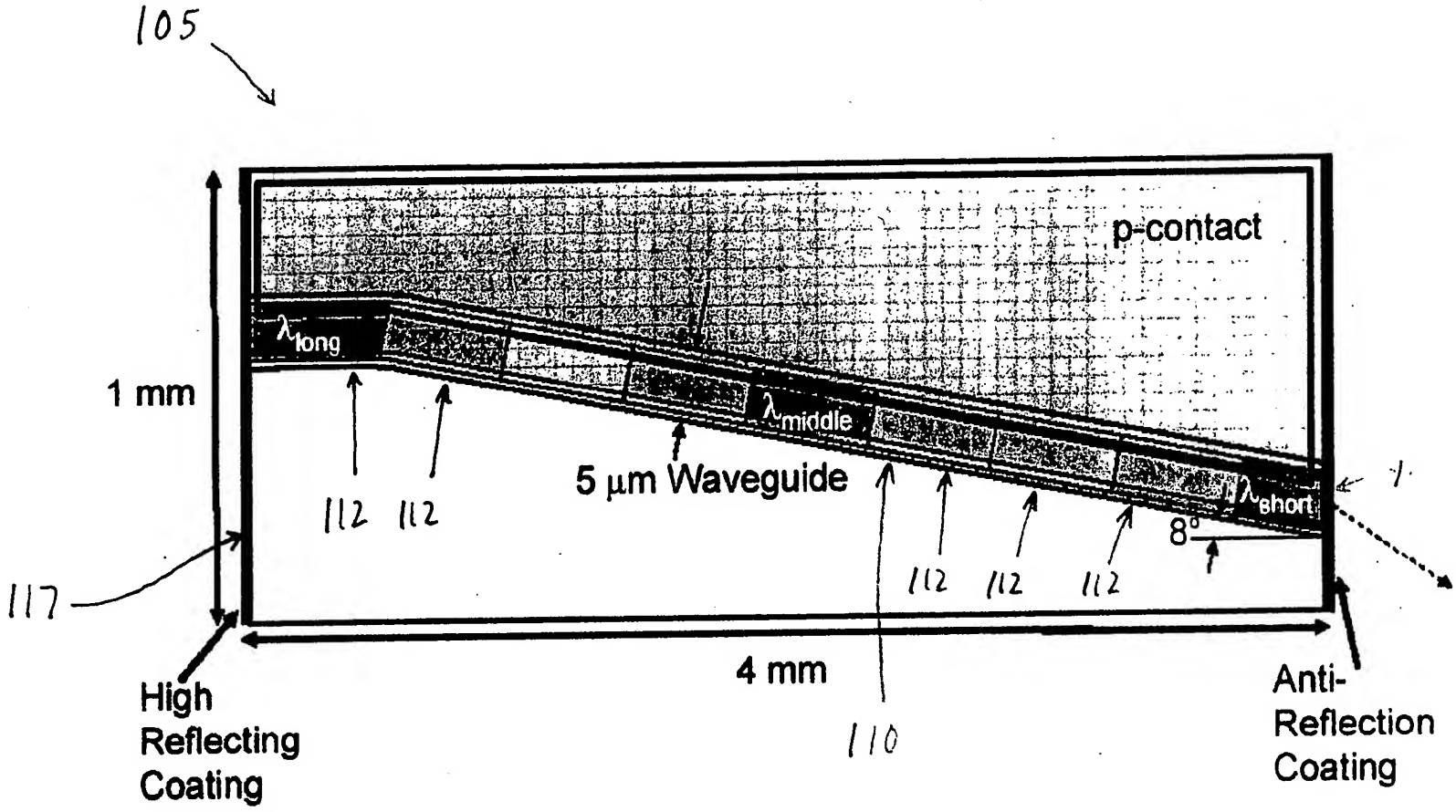


FIG. 8